CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A ~~configuration~~ circuit, comprising:

a program-controlled unit including an instruction execution pipeline having a plurality of pipeline stages;

said program-controlled unit ~~configured for~~ executing pipeline instructions instructing said program-controlled unit to stop an individual one of said plurality of pipeline stages, more than one of said plurality of pipeline stages, or all of said plurality of pipeline stages without creating any conditions for which one pipeline stage, a plurality pipeline stages, or all pipeline stages are stopped; and

the pipeline instructions stipulating which particular one of said plurality of pipeline stages or which particular ones of said plurality of pipeline stages should be stopped.

Claim 2 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein said program-controlled unit ~~is configured for~~ executes at least one of

said pipeline instructions specifying a length of time for which a respective one of said plurality of pipeline stages is to be stopped.

Claim 3 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein the instructions, which instruct stopping, or other instructions ~~can~~ stipulate a length of time for which a respective one of said plurality of pipeline stages is to be stopped.

Claim 4 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein said program-controlled unit ~~is configured for beginning~~ begins to stop a respective one of said plurality of pipeline stages at a particular time after executing an instruction that instructs stopping.

Claim 5 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein said program-controlled unit ~~is configured for beginning~~ begins to stop a respective one of said plurality of pipeline stages after an instruction that instructs stopping has passed through said instruction execution pipeline.

Claim 6 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein said program-controlled unit ~~is configured for setting~~ sets a time at which a respective one of said plurality of pipeline stages will begin to be stopped.

Claim 7 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein the pipeline instructions, which instruct stopping, or other instructions ~~can~~ stipulate a time for beginning to stop a respective one of said plurality of pipeline stages.

Claim 8 (currently amended). The ~~configuration~~ circuit according to claim 1, wherein, during normal operation, said program-controlled unit ~~is configured for blocking~~ blocks execution of the pipeline instructions, which instruct stopping.

Claim 9 (currently amended). The ~~configuration~~ circuit according to claim 8, wherein said program-controlled unit ~~is configured for treating~~ treats the pipeline instructions, which instruct stopping, as unknown instructions when execution of the pipeline instructions, which instruct stopping, is not enabled.